R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Cox for the indication of allowable subject matter.

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to generate a second reference signal in response to (i) a first reference signal and (ii) a timing signal, where a frequency and a phase of the second reference signal are (i) adjusted in response to the first reference signal and (ii) held when the first reference signal is lost. The second circuit may be configured to generate one or more output signals in response to the second reference signal and one of the one or more output signals, where the one or more output signals have a controlled and/or substantially zero delay with respect to the first reference signal.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the amendment to claims 1-2 and 13-14 can be found, for example, in FIGS. 2-4 as originally filed and, for example, in the specification on page 7, lines 2-11 and lines 16-18, page 8, lines 6-11, and page 9, lines 1-8 as originally filed. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-3, 5, 8-10, 13-15 and 19 under 35 U.S.C. §103(a) as being obvious over Graham et al. '797 (hereinafter Graham) in view of Ooishi '345 (hereinafter Ooishi) has been obviated by appropriate amendment and should be withdrawn.

Graham teaches a logic array having high frequency internal clocking (Title of Graham). Ooishi teaches a semiconductor device realizing an internal operational factor corresponding to an external operational factor stably regardless of fluctuations of the external operational factor (Title of Ooishi).

In contrast, presently pending claim 1 provides an apparatus comprising a first circuit that may be configured to generate a second reference signal in response to (i) a first reference signal and (ii) a timing signal. Claims 13 (means plus function) and 14 (method) provide similar recitations. Graham and Ooishi, alone or in combination, fail to teach or suggest a first circuit configured to generate a second reference signal in response to (i) a first reference signal and (ii) a timing signal, as presently claimed. As such, presently pending claims 1 and 13-14 are patentable over the cited references, alone or in combination, and the rejection should be withdrawn.

In particular, Graham teaches a low-skew clock buffer with zero delay between a clock signal (i.e., CLKIN) transition and

an output clock transition at terminals Q0-Q5 (see Graham at FIG. 7 and at column 9, lines 32-36). Graham fails to teach or suggest a circuit configured to generate a second reference signal in response to (i) a first reference signal and (ii) **a timing signal**, as presently claimed. Ooishi teaches (i) a difference adjusting circuit for detecting the difference in at a least one of phase and frequency between an external clock signal (i.e., extCLK) and an internal clock signal (i.e., intCLK) and for outputting a control potential for reducing the difference and (ii) a current control circuit for adjusting a driving current of the internal clock signal intCLK generating circuit in accordance with the control potential from the difference adjusting circuit. When the external clock signal extCLK is stopped, the output potential from the difference adjusting circuit is held (see Ooishi at FIG. 11 and Abstract). Ooishi fails to teach or suggest a circuit configured to generate a second reference signal in response to (i) a first reference signal and (ii) **a timing signal**, as presently claimed. Therefore, Ooishi fails to cure the deficiencies of Graham. As such, Graham and Ooishi, alone or in combination, fail to teach or suggest a circuit configured to generate a second reference signal in response to (i) a first reference signal and (ii) a timing signal, as presently claimed. As such, presently pending claims 1 and 13-14 are patentable over the cited references, alone or in combination, and the rejection should be withdrawn.

Claims 2-12 depend, directly or indirectly from claim 1 and claims 15-20 depend, directly or indirectly, from claim 14 which are believed to be allowable. As such, the presently pending invention is fully patentable over the cited references, alone or in combination, and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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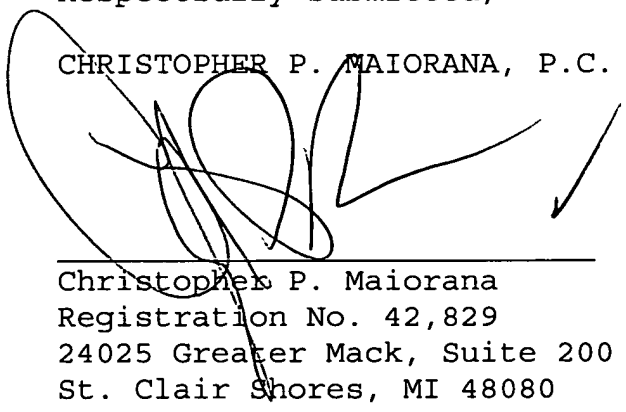

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

a first circuit configured to [receive a first reference signal and] generate a second reference signal in response to (i) a first reference signal and (ii) a timing signal, wherein a frequency and a phase of said second reference signal are (i) adjusted in response to said first reference signal and (ii) held when said first reference signal is lost; and

a second circuit configured to generate one or more output signals in response to said second reference signal and one of said one or more output signals, wherein said one or more output signals have a controlled and/or substantially zero delay with respect to said first reference signal.

2. (AMENDED) The apparatus according to claim 1, wherein said first circuit comprises:

a control circuit configured to generate a control signal in response to said first and second reference signals, wherein said control signal is held when said first reference signal is lost; and

an oscillator configured to generate said second reference signal in response to said control signal and said timing signal.

13. (AMENDED) An apparatus for generating one or more output signals comprising:

means for [receiving a first reference signal and] generating a second reference signal in response to (i) a first reference signal and (ii) a timing signal, wherein a frequency and a phase of said second reference signal are (i) adjusted in response to said first reference signal and (ii) held when said first reference signal is lost; and

means for generating said one or more output signals in response to said second reference signal and one of said one or more output signals, wherein said one or more output signals have controlled and/or substantially zero delay with respect to said first reference signal.

14. (AMENDED) A method of generating one or more output signals comprising the steps of:

(A) [receiving a first reference signal and] generating a second reference signal in response to (i) a first reference signal and (ii) a timing signal, wherein a frequency and a phase of said second reference signal are (i) adjusted in response to said first reference signal and (ii) held when said first reference signal is lost; and

(B) generating said one or more output signals in response to said second signal and one of said one or more output

signals, wherein said one or more output signals have controlled and/or substantially zero delay with respect to said second reference signal.